IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VIASAT, INC., **Plaintiff,** **vs.** **WESTERN DIGITAL CORPORATION and WESTERN DIGITAL TECHNOLOGIES, INC.,** **Defendants.**	**Case No.: 6:21-cv-01230-ADA** **JURY TRIAL DEMANDED**
VIASAT, INC., **Plaintiff,** **vs.** **KIOXIA CORPORATION and KIOXIA AMERICA, INC.,** **Defendants.**	**Case No.: 6:21-cv-01231-ADA** **JURY TRIAL DEMANDED**

PLAINTIFF'S RESPONSE TO DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

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I. Introduction

Viasat's proposed construction of the disputed terms in the '700 and '347 patents properly conform to the plain and ordinary meaning of those terms as understood by a person of ordinary skill. Defendants, on the other hand, contort both the record and reality to squeeze well-understood structural terms—like "error detection sub-module" and "error correction module"—into the ill-fitting box of means-plus-function claiming. Defendants' inadequate theory of indefiniteness fails on its face and stands in stark contradiction to the positions these same Defendants have taken in front of the PTAB on these same patents—attacks in which the Defendants have given zero notice to the PTAB that they believe the asserted patents' language is, in any way, indefinite. Defendants' remaining constructions are infringement-directed efforts to promote proposed constructions unsupported by the intrinsic evidence and inconsistent with the plain and ordinary meaning. The Court should reject them too.

II. Level of Ordinary Skill in the Art

A POSA would have had at least a B.S. in electrical engineering, computer engineering, or computer science or a related field, and at least two years of experience in the design, development, or research of the hardware implementation of error correction systems. Ex. 1, Declaration of Nader Bagherzadeh, Ph.D. ("Bagherzadeh Decl.") ¶¶ 61-67. Advanced education may substitute for experience and vice versa. *Id.* ¶ 64.

III. '700 Patent

A. The proper construction of "*decode the received encoded data to generate a plurality of partially decoded data streams*" based on the intrinsic evidence is "process the received encoded data to generate more than one data stream for error detection"

Viasat construes the term "decode the received encoded data to generate a plurality of partially decoded data streams" the way a POSA would understand the term in the context of the

patent specification—"process the received encoded data to generate more than one data stream for error detection." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) ("Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.").

Defendants say that Viasat is "broadening" the term by substituting "process" for "decode." But Defendants ignore the intrinsic evidence. Far from broadening, Viasat's construction adopts the exact language used in the specification to describe what it means to "partially decode." The specification states expressly (in a passage never cited by Defendants) that the decoding module receives the encoded data and may "process" the data to "generate a number of data streams." Ex. 2, U.S. Patent No. 8,615,700 at 6:9-11. This processing is what generates, in one embodiment, the plurality of "decoded (or partially decoded) data streams." *Id.* at 6:11-14.

> The decoder module 205 may receive encoded data from flash memory, and **process the received encoded data to generate a number of data streams**. In one embodiment, the decoder module processor may buffer, de-interleave, or perform certain aspects of the decoding process, **an[d] thereby generate decoded (or partially decoded) data streams**.

Id. at 6:9-14; *see also id.* at Fig. 5. Viasat's construction accurately captures what is disclosed in the specification. Defendants ignore it.

Defendants have a second problem. Not only do they ignore what's clear from the specification, but they also advance a construction and arguments that are inconsistent with the claim construction they are currently pressing for in the PTAB. Defendants tell this Court that Viasat's construction is impermissibly broad because it would improperly encompass the mere buffering of a data stream. Defs.' Op. Br. at 3.

To the PTAB, however, the Defendants say the opposite. There, Kioxia contends expressly that this claim term would be understood by a POSA to include "buffer[ing] the received encoded

data" and that buffering alone is sufficient to "decode." Ex. 3, Kioxia '700 Patent IPR Petition at 14-15.

> The plain and ordinary meaning of the term "decode the received encoded data to generate a plurality of partially decoded data streams" is "**buffer the received encoded data**, de-interleave the received encoded data, or distinguish error correction bits from information bits in the received encoded data, **to generate a plurality of data streams**." This construction is consistent with the way the term . . . is used in the '700 Patent as understood by a POSITA. ['700 patent] at 6:11-14.

Id. Defendants advance one interpretation of the intrinsic evidence when it suits them in front of the PTAB and another one here.

Even setting aside their about-face, Defendants' criticisms are also based on a misreading of Viasat's construction. Viasat has never contended that routine buffering alone is sufficient to satisfy this element. Viasat's construction makes clear that the claim requires more: the decoding module must (1) *process* the received encoded data to (2) *generate* more than one data stream (3) *for* error detection. Routine buffering is not enough. And that's consistent with the intrinsic record, which does not say that buffering alone is sufficient, but rather that the decoding module may include some buffering steps when generating a plurality of partially decoded data streams. *See* Ex. 2 at 6:9-14 ("the **decoder module processor** may buffer, de-interleave, or perform certain aspects of the decoding process, an[d] thereby generate decoded (or partially decoded) data streams").

Defendants' concern that Viasat's construction would cover "demodulation" is even further off the mark. Demodulation refers to the process of recovering a data signal from a modulated carrier wave (e.g., a radio wave)—something present in over-the-air data transmissions and exclusive to data transmission that uses modulation, like satellite communication. Bagherzadeh Decl. ¶ 108. There is no modulation (and thus no demodulation) in the process of reading out, and decoding, data stored in a flash memory device. *Id.*

Viasat's statements to the Patent Office regarding the Suzuki patent publication are thus consistent with its construction. Viasat merely told the Patent Office that Suzuki's "demodulation" of a single data stream (in the context of beamed satellite communications) is not the same as decoding to generate a plurality of partially decoded data streams in a flash memory device. Defs.' Ex. 3 at 10. No POSA would confuse these two ideas. And as noted to the Patent Office, Suzuki is also readily distinguishable in that it does not involve decoding to generate a **plurality** of partially decoded data streams—it involves a single stream of transmitted satellite data. *Id.*

Finally, contrary to Defendants' suggestion, Viasat's construction includes the phrase "for error detection" for clarity. That phrase does not import a limitation from the specification—the error detection aspect is in the claim itself, as Defendants agree. Defs.' Op. Br. at 3. The "error detection module" receives the partially decoded data streams and then performs error detection. Ex. 2 at 10:50-59. For the same reasons, the phrase is not redundant. All "for error detection" does is link the generation of partially decoded data streams to the next set of claim limitations involving error detection.

B. "*Error detection sub-modules*" is readily understandable as a definite structure according to its plain and ordinary meaning

Defendants have cherry-picked a select number of "module"[1] terms from the '700 and '347 patents for purposes of an indefiniteness attack, in which they elide the well-understood structural understanding of these terms and instead propose construing them as means-plus-function claims

[1] Some of the terms in question are "module" terms and some are "sub-module," a distinction that creates no significant nuance or difficulty in their construction. Both terms are used in the patent claims (and Defendants assert no indefiniteness argument against error detection module). A POSA would recognize, for example, that an error detection module structure could comprise multiple error detection sub-modules. Bagherzadeh Decl. ¶ 77.

under 35 U.S.C. § 112, ¶ 6. But none of these terms are the generic "black box" of pure function that Defendants try to conjure.

A POSA would understand the term "error detection sub-modules" to "have a sufficiently definite meaning as the name for structure." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (*en banc*). "The ultimate question is whether 'the claim language, read in light of the specification, recites sufficiently definite structure to avoid § 112, ¶ 6.'" *MTD Prods. Inc. v. Iancu*, 933 F.3d 1336, 1342 (Fed. Cir. 2019) (citations omitted).

Error detection sub-module is such a term. It requires no construction and can be understood according to its plain and ordinary meaning. A POSA readily and easily understands that it is the structural component containing the circuitry on the chip (ASIC or otherwise) that identifies the existence of an error in a chunk of data read from the flash memory. Bagherzadeh Decl. ¶ 75. No further construction is required.

Defendants' efforts to shoehorn this term into the category of means-plus-function fails. First, the claim does not use the word "means." The absence of the word "means" in the claim language creates a presumption that the term is not means-plus-function claiming—a presumption Defendants can rebut, but only if they overcome it by a preponderance of the evidence. *See, e.g.*, *Rasmussen Instruments, LLC v. DePuy Synthes Prods., Inc.*, 568 F. Supp. 3d 117, 123 (D. Mass. 2021). Defendants have failed to meet their burden here.

First, Defendants try to paint the use of the word "module" as itself evidence that the presumption against indefiniteness is overcome. But there is nothing about using the word "module" that inherently weighs against the presumption here, and courts have repeatedly found "module" terms that denote sufficiently definite structure to be outside § 112, ¶ 6. *See, e.g.*, Claim Constr. Order at 33, 39, 40, *ParkerVision, Inc. v. LG Elecs., Inc.*, No. 6:21-cv-520-ADA (W.D.

Tex. June 21, 2022), ECF No. 55 (construing multiple "module"-containing claims as not means-plus-function, including "frequency down-conversion module" (at 33), "a down-convert and delay module" (at 39), and "at least one delay module" (at 40)); *Modern Font Applications LLC v. Red Lobster Hospitality LLC*, No. 6:21-CV-470-ADA, 2022 WL 659396, at *9-11 (W.D. Tex. Mar. 4, 2022) (construing "exposure module" and "program module" without reference to any means-plus-function eligibility); *IPCom GmbH & Co. KG v. AT&T Corp.*, No. 2:20-CV-00322-JRG, 2021 WL 4191407, at *24-25 (E.D. Tex. Sept. 15, 2021) (finding "transmission radio module" denotes a known class of structures and is not governed by § 112, ¶ 6); *Microchip Tech. Inc. v. Nuvoton Tech. Corp. Am.*, No. 19-cv-01690-SI, 2020 WL 978636, at *8-12 (N.D. Cal. Feb. 28, 2020) (construing disputed claims "interface module," "serial engine module," and "port control module" as not governed by § 112, ¶ 6); *SAS Inst. Inc. v. World Programming Ltd.*, No. 2:18-cv-295-JRG, 2020 WL 569856, at *15-16 (E.D. Tex. Feb. 5, 2020) (finding "graph generator module" not means-plus-function based on surrounding claim language that "inform[ed] the structural character" and use in the field to denote structure).

The fact that the term includes functional language as a modifier (whether "error detection" or "error correction") does not turn the claim term into a means-plus-function claim and overcome the presumption. *See, e.g., Zeroclick, LLC v. Apple Inc.*, 891 F.3d 1003, 1008 (Fed. Cir. 2018) (noting that "the mere fact that the disputed limitations incorporate functional language does not automatically convert the words into means for performing such functions"); *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed. Cir. 1996) ("Many devices take their names from the functions they perform. The examples are innumerable, such as 'filter,' 'brake,' 'clamp,' 'screwdriver,' or 'lock.'"). To the contrary, "error detection sub-module" would evoke in the mind

of a POSA definite structures within a computer chip's hardware architecture, and not merely functions to be performed on a generic device. Bagherzadeh Decl. ¶¶ 79-87.

Ultimately, the "question whether the [claim term] invokes § 112, ¶ 6, depends on whether persons skilled in the art would understand the claim language to refer to structure, assessed in light of the presumption that flows from the drafter's choice not to employ the word 'means.'" *Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp.*, 948 F.3d 1342, 1354 (Fed. Cir. 2020). Here, the intrinsic evidence, including the surrounding claim language and the specification, "inform[s] the structural character" of an error detection sub-module as a definite structure and not purely functional. *SAS Inst.*, 2020 WL 569856, at *15-16.

Claim 1 describes the error detection module, comprised of error detection sub-modules, in its physical context and connectivity relative to the other components of the claimed flash memory decoder. The error detection module, with its sub-modules, is "communicatively coupled" to the decoding module. Ex. 2 at 10:52-53; Bagherzadeh Decl. ¶ 89. That same error detection module is also "communicatively coupled" to the error correction module but required to be "physically separate." Ex. 2 at 10:62-63; Bagherzadeh Decl. ¶ 90. The error detection sub-modules are connected such that they will "forward" the relevant data in which an error was detected to the error correction module. Ex. 2 at 10:60-61; Bagherzadeh Decl. ¶ 90. Taken together, a POSA reading the '700 patent would understand "error detection sub-module" to describe a class of definite structures for error detection. Bagherzadeh Decl. ¶¶ 89-90.

Defendants' construction of the "physically separate" limitation confirms the structural nature of the different "module" claim terms. For that limitation, Defendants acknowledge that the error correction module and error detection module are implemented in hardware circuitry. Defs.' Op. Br. at 16-18. Viasat agrees with that premise—the error detection module and error correction

modules are physical structures deployed in hardware. (As explained below, Viasat disagrees with other aspects of Defendants' "physically separate" construction, which is unduly narrow.)

The structural character of the error detection sub-modules is also confirmed by the specification. Bagherzadeh Decl. ¶¶ 92-94. For example, the figures in the patent, like Figure 3, place the error detection sub-modules in their structural context relative to the other components in an arrangement of physical structures. Ex. 2 at Figure 3; Bagherzadeh Decl. ¶ 92. Figure 3 includes a number of other components that are unquestioned physical structures, like the "Encoder," the "Controller," and the "Sector(s)" of the flash memory storage itself that are connected to and placed relative to decoding sub-modules. *Id.*

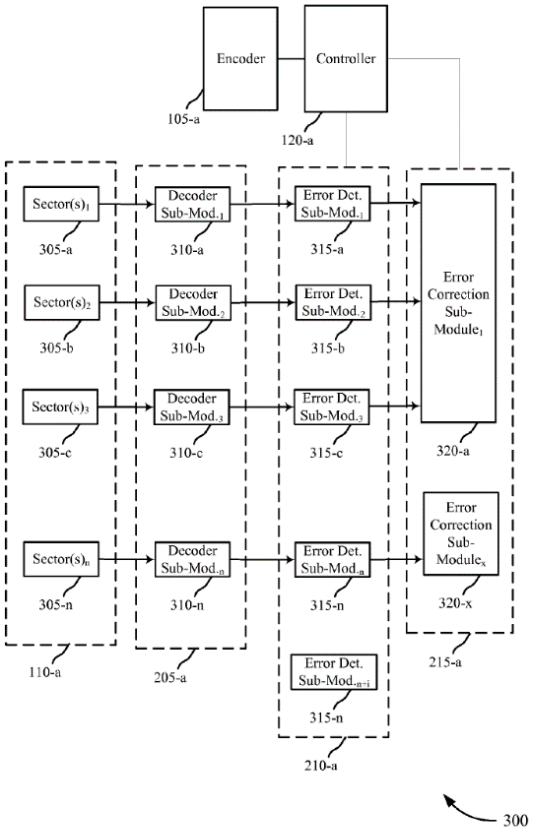

FIG. 3

The structural context is further buttressed by the specification's note that these systems can be "implemented with one or more Application Specific Integrated Circuits (ASICs) adapted

to perform some or all of the applicable functions in hardware." Ex. 2 at 3:31-36, 5:62-65; Bagherzadeh Decl. ¶ 94. ASICs are known custom integrated circuits whose physical architecture is designed for a specific target application—in this case for error detection and correction of data read from flash memory. Bagherzadeh Decl. ¶¶ 53-56, 94. A POSA reading the claims in this context, and familiar with the need in modern flash memory to maximize performance and power efficiency, would have a clear understanding that the error detection sub-modules reflect a definite structural component of the flash memory decoder. *Id.*

The specification also provides specific and well-known error correcting algorithms that "may be used" for error detection and correction based on the patent—for example, Bose Chaudhuri Hocquenghem (BCH) codes, Reed Solomon (RS) codes, or low-density parity check codes (LDPC). Bagherzadeh Decl. ¶¶ 28-37, 95-97; Ex. 2 at 4:7-28. A POSA knows that these algorithms require certain structures for error detection and correction, and therefore naming those algorithms necessarily describes a class of definite structures implemented in hardware. Bagherzadeh Decl. ¶¶ 95-97. The literature of the field is replete with references that describe the use of these codes as definite physical structures for error detection and correction. *Id.*; *see also* Ex. 4, A.J.A. Antunes, *Verilog Implementation of a Forward Error Correcting Reed Solomon Encoder and Decoder* (2017) (describing use of Reed-Solomon in decoder with "error detection module" and "error correction module"); Ex. 5, H. Lee, *High-Speed VLSI Architecture for Parallel Reed-Solomon Decoder* (2003) (same); Ex. 6, B. Huang, *An Area Efficient Multi-Mode Architecture for Reed-Solomon Decoder* (2009) (describing use of BCH as definite physical structure with specific "modules"). Intrinsic evidence of the '700 patent—the Chen 2008 article describing the use of BCH codes—says the same. Bagherzadeh Decl. ¶ 96; Ex. 7, B. Chen, *Error Correction for Multi-Level NAND Flash Memory Using Reed-Solomon Codes* (2008).

Consistent with its usage in the intrinsic record, a POSA would readily recognize that the term error detection sub-module reflects common parlance to describe a known class of structures in error correction systems. *See Skky, Inc. v. MindGeek, s.a.r.l.*, 859 F.3d 1014, 1019 (Fed. Cir. 2017) (finding "wireless device means" not a means-plus-function term, noting that "it is sufficient if the claim term is used in common parlance or by persons of skill in the pertinent art to designate structure, even if the term covers a broad class of structures and even if the term identifies the structures by their function"); *IPCom*, 2021 WL 4191407, at *24-25 (finding "transmission radio module" denotes a known class of structures and is not governed by § 112, ¶ 6); Bagherzadeh Decl. ¶¶ 79-87. That is why "error detection module" appears throughout the extrinsic evidence to describe definite structures that detect errors. Bagherzadeh Decl. ¶¶ 79-87; *see, e.g.*, Ex. 8, M. Ashouei, *Improving SNR for SDM Linear Systems Using Probabilistic Error Correction and State Restoration: A Comparative Study* (2006) at Fig. 1 (diagramming physical structure of an error correction system that includes an "error detection module" structure); Ex. 5 at Fig. 1, Table II, Fig. 7 (identifying "error detection" module and submodule structures).

And it is also generally recognized in this field that error detection, however specifically named, is performed by definite structural elements. Bagherzadeh Decl. ¶¶ 84-86; *see, e.g.*, Ex. 6 at Fig. 2 (denoting error detection done, at least in part, by structural feature of the Syndrome Calculate module). The intrinsic evidence is consistent with this. For example, the "Micron Technology Inc. ECC Module for Xilinx Spartan-3" datasheet, referred to on the front of the patent, details the structure of an "ECC Module for NAND Flash," including the specific types of physical logic gates used for error detection and correction. Ex. 9 at 16-17 ("To detect and correct errors, the two sets of 24-bit Hamming codes are XOR'ed to find the result."); Bagherzadeh Decl. ¶¶ 54, 96 (describing XOR gates as physical structures known to persons of skill).

As a term of art commonly denoting structural components—and used in that same way in the '700 patent—error detection sub-module is not a means-plus-function claim term. *See Microchip Tech.*, 2020 WL 978636, at *9-11 (finding "serial engine module," and "port control module" not governed by § 112, ¶ 6 in part because extrinsic evidence showed they were terms of art denoting structure).

The Court need not go further to reject Defendants' arguments. But it is also highly probative that Defendants' position here that the term error detection sub-module (and the other disputed "module" terms) is indefinite directly contradicts their positions before the PTAB. *See* Ex. 3 at 14; Ex. 10, Western Digital '700 Patent IPR Petition at 20; Ex. 11, Western Digital '347 Patent IPR Petition at 21. The Board will not institute IPR if it finds that a claim term is indefinite. If it "cannot ascertain the scope of a claim with reasonable certainty for purposes of assessing patentability," the Board must "decline to institute the IPR or, if the indefiniteness issue affects only certain claims, to conclude that it could not reach a decision on the merits with respect to whether petitioner had established the unpatentability of those claims under sections 102 or 103." *Samsung Elecs.*, 948 F.3d at 1353.

The IPR petitions never suggest that Defendants think any of the terms are subject to § 112, ¶ 6 or indefinite. Kioxia instead represents to the Board that "Petitioner interprets the claims 'in accordance with the ordinary and customary meaning . . . as understood by one of ordinary skill in the art.'" Ex. 3 at 14 (citation omitted). Likewise, Western Digital states that "[t]his Petition construes terms consistent with the understanding a POSA would have had, at the time of the

invention, in view of the [] patent's intrinsic evidence and, where appropriate, extrinsic evidence." Ex. 10 at 20; Ex. 11 at 21.[2]

Throughout their IPR petitions, Defendants present detailed arguments based on their understanding of the structure of the various "module" terms in the claims of the '700 and '347 patents and assert that a POSA would find those structures in the prior art. Defendants showed no difficulty cracking open the supposedly "generic black boxes" of the error detection sub-modules (or any of the "module" terms) and mapping that language onto the prior art. Indeed, Defendants even mix-and-match various structures found within modules of the asserted prior art in an effort to cobble together an invalidity case. This would be impossible to do if these modules were, as they now protest before this Court, indefinite and purely functional "black boxes" descriptions. The Court should not countenance this type of behavior.

Finally, even if the Court finds the term error detection sub-module is governed by § 112, ¶ 6, the '700 patent discloses corresponding structures for the claimed function. The specification describes in detail how the error detection sub-modules receive one of the plurality of partially decoded data streams, detect whether there is an error in the data stream, and forward the portion of the respective received stream containing an error to an error correction module. *See, e.g.*, Ex. 2 at Figs. 3-5, 6:29-8:61. The specification also discloses a number of well-known and understood error correction codes—e.g., BCH, LDPC, RS, and turbo codes. *Id.* at 4:7-24. While the

[2] Defendants clearly recognize the irreconcilable conflict between their positions before this Court and the PTAB. They sought to cabin and minimize the impact of their positions before the PTAB with hedging language, which outlines the impossible undertaking of "merely" identifying prior art disclosures as falling clearly within (and thus anticipating) claims that Defendants tells this Court are indefinite. *See, e.g.*, Ex. 10 at 20 ("Further, by identifying disclosure in the prior art as meeting certain claim limitations Petitioner merely asserts that the scope of such limitation, even if indefinite, and if not limited by 35 U.S.C. § 112 ¶ 6, would at least include the identified disclosure.").

mathematical formulas underlying these codes are complex, they were known to a POSA at the time. Bagherzadeh Decl. ¶¶ 98-99. These codes were all specifically designed to perform the functions of detecting and correcting errors in data, and a POSA would readily understand how to adapt the error correction codes identified in the specification to implement the claimed functions of the error detection sub-modules of the invention as described in the specification. *Id.* Thus, the detailed disclosure in the specification of the steps required to perform the claimed invention—in combination with the specific error correction codes listed in the specification—disclose an algorithmic structure for performing the claimed functions of the error detection sub-modules.

C. The plain and ordinary meaning of the claim term "*operating in parallel*" is understood without any further construction

The term "operating in parallel" is a term easily understood according to its plain and ordinary meaning without any further construction. *Phillips*, 415 F.3d at 1312-13. Kioxia's proposed construction, on the other hand, is an unjustified effort to narrow the meaning of the term with no support from the language or the intrinsic and extrinsic evidence. (Indeed, not even Western Digital signs onto Kioxia's construction. *See* Defs.' Op. Br. at 10 n.5.)

Operating in parallel is simple. It means the modules in question are operating in a parallel fashion, as opposed to serially. The prosecution history cited by Kioxia makes exactly this point—the actions described by Suzuki were done in a serial fashion as opposed to the parallel operation claimed in the '700 patent. Defs.' Ex. 3 at 11.

> The claimed error detection module comprises a plurality of error detection submodules performing the **same functions and operating in parallel**, whereas in Suzuki, the various functional blocks (e.g., the demodulator, blocks of the FEC decoding chain, the CP processor) perform **different functions and operate serially**.

Id.

Kioxia looks to narrow the plain and ordinary meaning to a specific example of how modules may operate in parallel—"at the same time." But parallel operation is not so limited. For example, it is easily understood that two surgeons operating in two surgical rooms will "operate in parallel," even though one surgeon may begin first and the other may end later. Parallel operation—whether in surgery or in flash—allows for incomplete overlap. And that stands in clear contrast to two surgeons operating serially in a single surgical room—the second surgeon must wait for the first surgery to be completed before the second surgery occur. No overlap is possible.

Nothing in the intrinsic evidence supports adopting Kioxia's narrow view of the limitation. The only intrinsic evidence Kioxia points to confirms Viasat's point—that operating in parallel simply is the opposite of operating serially. *Id.* And Kioxia's extrinsic evidence talks of parallel processing as concurrent *or* simultaneous in nature, the former of which refers to overlapping spans of time. Defs.' Ex. 4 at WD-Viasat-WDTX00026407. That is, two things operating in parallel need not begin or end at the same time.

Lastly, Kioxia pleads that the jury will be confused without a construction. But it does not help a jury to limit the claims in a way that is incorrect and unsupportable. And there's no reason to believe a jury will be unable to grasp the plain and ordinary meaning of "operating in parallel." It is a straightforward concept that witnesses will surely be able to explain to the jury.

D. "*Error correction module*" is readily understandable as a definite structure according to its plain and ordinary meaning

For many of the same reasons identified above with the term "error detection sub-modules," the term "error correction module" is easily understood to a POSA as describing a definite structure and not subject to construction as a means-plus-function claim term. *See* § III.B, *supra*. It requires no construction and can be understood according to its plain and ordinary meaning. A POSA readily and easily understands that it is the structural component containing the

circuitry on the chip (ASIC or otherwise) that corrects an error detected in a chunk of data read from the flash memory. Bagherzadeh Decl. ¶ 76. No further construction is required.

Error correction module is not a generic black box term governed by § 112, ¶ 6. As with error detection sub-modules, the claim does not use the word "means" and is therefore presumed as not means-plus-function. Neither the use of the word "module" nor functional modifying language overcomes that presumption. *See, e.g.*, *Zeroclick*, 891 F.3d at 1008.

Also as with error detection sub-module, error correction module is used in the claim with surrounding language that "inform[s] the structural character" of the term. *SAS Inst.*, 2020 WL 569856, at *15-16. It is "communicatively coupled" to the error detection module but "physically separate." Bagherzadeh Decl. ¶ 90; Ex. 2 at 10:62-63. The error correction module is connected to the error detection sub-modules such that those sub-modules will "forward" the relevant data in which an error was detected to them. Ex. 2 at 10:60-61; Bagherzadeh Decl. ¶ 90.

The structural character of the error correction module is confirmed by the specification and the intrinsic evidence. Figure 3 shows an arrangement of physical structures in one embodiment, with error correction modules depicted in their structural context relative to the other components. Ex. 2 at Fig. 3. And multiple statements in the specification note that the inventive systems can be "implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware." *Id*. at 3:31-36, 5:62-65; Bagherzadeh Decl. ¶ 94. Moreover, the specification specifically invokes and describes the use of well-known error correction code algorithms like BCH, RS, and LDPC, which a POSA would recognize as describing specific structures in an error correction system's hardware, and not merely functions to be performed on a generic device. Ex. 2 at 4:7-28; Bagherzadeh Decl. ¶¶ 95-97. Given these disclosures, a POSA reading the '700 patent would understand "error

correction module" to be structural, referring to a class of definite structures for error detection. Bagherzadeh Decl. ¶ 88.

This structural understanding of the term is also borne out in the extrinsic evidence. A POSA would readily recognize that error correction module is a common way for persons of skill in this art to describe a known class of structures in error correction systems. Bagherzadeh Decl. ¶ 79; *Skky*, 859 F.3d at 1019. That is why "error correction module" appears throughout the extrinsic evidence to describe a physical structure that corrects errors. Bagherzadeh Decl. ¶¶ 80-87; *see also, e.g.*, Ex. 8 at Fig. 1 (diagramming circuit of error correction module); Ex. 5 at Fig. 1, Table II, Fig. 7; Ex. 6 at Fig. 5 (showing the "Basic Cell of Error Correction module"); *see also* Ex. 12, S.A. Abbasi, *FPGA Based Realization of a Reduced Complexity High Speed Decoder for Error Correction* (2003) at Viasat_FEC_00002115 (describing in the "Hardware Implementation" section the "Error-Correction Module"), Viasat_FEC_00002114 (calling out "the error corrector **circuit**"). As a term of art commonly denoting structural components, error correction module is not a means-plus-function claim term. *See Microchip Tech. Inc.*, 2020 WL 978636, at *10-11.

Finally, as with the other module terms in the asserted patents, Defendants have taken a wholly inconsistent position on error correction module in front of the PTAB. That Defendants evidently had no trouble identifying specific structures for "error correction modules" in the prior art proves the point—this term is easily understood to be a structural one.

However, even if the Court finds the term error correction module is governed by § 112, ¶ 6, the '700 patent discloses corresponding structures for the claimed function. The specification describes in detail how the error correction module is configured to correct the received portions of the respective received streams containing an error. *See, e.g.*, Ex. 2 at Figs. 3-5, 6:29-8:61. The

specification also discloses a number of well-known and understood error correction codes—e.g., BCH, LDPC, RS, and turbo codes. *Id.* at 4:7-24. While the mathematical formulas underlying these codes are complex, they would be known to a POSA at the time. Bagherzadeh Decl. ¶¶ 98-99. These codes were all specifically designed to perform the functions of detecting and correcting errors in data, and a POSA would readily understand how to adapt the error correction codes identified in the specification to implement the claimed functions of the error correction module of the invention as described in the specification. *Id.* Thus, the detailed disclosure in the specification of the steps required to perform the claimed invention—in combination with the specific error correction codes listed in the specification—discloses an algorithmic structure for performing the claimed functions of the error correction module.

E. Kioxia's proposed construction of "*forward the portion of the respective received stream containing an error to an error correction module*" improperly alters the plain and ordinary meaning in a manner inconsistent with the intrinsic record

Viasat's proposed construction—"communicate the data in which an error was detected from the error detection submodule to an error correction module"—more accurately captures the specific meaning of the word "forward" and avoids any possible confusion based on the word's usage in different contexts (e.g., "forward error correction"). Both the claims and specification correlate "forward" with "communicate."

In claim 1 itself, the error correction module is "communicatively coupled" with the error detection module. When the error detection module "forward[s] the portion of the respective received stream containing an error to an error correction module," it is communicating that data in which an error was detected to the error correction module.

The specification reiterates that forwarding and communication are related:

- "Each of these system 100 components may be in **communication** with each other." Ex. 2 at 3:31-32.

- "An embodiment of the decoder 115 includes an error correction module in **communication** with and physically separate from an error detection module." *Id.* at 3:49-52.

- "The flash memory decoder 115-a includes a decoder module 205, an error detection module 210, and an error correction module 215, and each of may be in **communication** with each other." *Id.* at 5:52-55.

- "The flash memory decoder system 300 includes flash memory 110-a, a decoder module 205-a, an error detection module 210-a, an error correction module 215-a, a controller 120-a, and an encoder 105-a. Each of these components may be in **communication** with each other." *Id.* at 6:33-38.

Kioxia argues that "communicate" is somehow "ambiguous and unbounded." Defs.' Op. Br. at 16. But "communicate" is an easily understood and clear word, repeatedly used in the claims and specification. Nothing about the word—especially within the context of the specification and claim term—permits the "unbounded" communication of other information about the data (e.g., metadata) without forwarding the actual data itself. To even state Kioxia's argument that "communicate the data" would somehow cover a situation where no data is actually forwarded is to recognize its absurdity.

Similarly, there is nothing broadening about Viasat's proposal that the relevant data is "data in which an error was detected." It merely identifies the specific data (i.e., "the portion of the respective received stream containing an error") being communicated more precisely. In contrast, Kioxia's construction fails to give any meaning to "the portion of the respective received stream," instead collapsing that entire phrase into the word "data." And the suggestion that Viasat's construction allows communication of data without any error, where the error was already corrected, defies the very words of the claim—data is not corrected until it has been forwarded to an error correction module.

F. Defendants import unsupported limitations to narrow "*error correction module, . . . physically separate from [the/an] error detection module*" beyond its plain and ordinary meaning

The term "error correction module, . . . physically separate from [the/an] error detection module" (and specifically "physically separate") is a term easily understood according to its plain and ordinary meaning without any further construction. *Phillips*, 415 F.3d at 1312-13. It means what it says—the error correction module and error detection module are physical structures, which are separate from each other. Neither the plain meaning of the words "physically separate" nor the intrinsic record supports Defendants' construction requiring "employing only circuitry that is not employed by the error detection module." Rather, Defendants misread the prosecution history and the specification.

Defendants rely on a statement in the prosecution history distinguishing Viasat's invention from the prior art of Suzuki. Defendants say that Viasat argued the Suzuki embodiment at issue was "operating on a single integrated circuit." Defs.' Op. Br. at 17. Not so. Viasat told the Patent Office that Suzuki taught "conventional turbo decoding and RS decoding, wherein error detection and error correction for the respective FEC code is not performed by modules which are physically separate." Defs.' Ex. 3 at 11-12 (discussing Defs.' Ex. 7 at [0142] and Fig. 18B). Viasat did not, as Defendants argue, distinguish Suzuki based on any teachings about implementation within a single integrated circuit. Indeed, Viasat did not even mention the word "circuit" when distinguishing Suzuki. *Id.*

And Suzuki does not restrict itself to a single circuit, contrary to Defendants' suggestion. Defs.' Op. Br. at 17. At best, Suzuki says that one embodiment of a satellite receiver set-top box includes an advanced modulation receiver that "**may** be implemented within a single integrated circuit." Defs.' Ex. 7 at [0073]. But of course, that leaves open the possibility that embodiments can be implemented in multiple integrated circuits. *See also id.* at [0112] (devices "may be

implemented using one or more integrated circuits"). Suzuki's teachings underline that Viasat was not distinguishing its invention from Suzuki based on it purportedly being implemented on a single integrated circuit.[3]

Defendants fare no better by citing places in the specification that use the word "circuit" and claiming that "confirms" their proposed construction. That the specification notes the invention can be implemented on types of "circuits" is unremarkable for this type of invention, and uninformative as to the meaning of "physically separate." It certainly cannot modify its plain and ordinary meaning. And Defendants completely gloss over the fact that the very nature of their construction of physically separate bears on the "module" terms. Defendants here rely on specific invocations of circuitry in the specification, implicitly acknowledging the definite structural aspects of the error correction and detection modules. Defendants make no attempt to reconcile the conflict between the "physically separate" construction and their position that the module terms are somehow purely functional and indefinite.

Defendants' extrinsic evidence does not move the needle. Those dictionary definitions merely confirm the truism that separate doesn't mean together.

G. "*Error monitoring module*" is readily understandable according to its plain and ordinary meaning as a definite structure for counting errors in an error correction system

The term "error monitoring module" is easily understood by a POSA as describing a definite structure. It requires no construction and can be understood according to its plain and

[3] Defendants' proposed construction is itself unclear about whether it purports to require the modules be on separate integrated circuits (i.e., computer chips) when they reference different "circuitry." Nothing in the intrinsic or extrinsic evidence they cite speaks to this either. This added layer of unnecessary ambiguity is yet another reason not to deviate from the plain and ordinary meaning of the words of the claim.

ordinary meaning. A POSA readily and easily understands it is a structure that counts errors over time in an error correction system. Bagherzadeh Decl. ¶ 101. No further construction is required.

Error monitoring module is not a generic black box term that requires construction as a means-plus-function term. As discussed in Sections III.B and III.D, *supra*, this term does not use the word "means" and is therefore presumed not to invoke means-plus-function claiming. Nor does the word "module" nor the functional modifier overcome that presumption. *See, e.g.*, *Zeroclick*, 891 F.3d at 1008.

The surrounding language of the claims provide context that "inform[s] the structural character" of the term. *SAS Inst.*, 2020 WL 569856, at *15-16. As with the error detection sub-modules and error correction module, the claims describe the structural configuration of the error monitoring module and its connections with other modules. *See* Sections III.B and III.D, *supra*. For example, the error monitoring module is "communicatively coupled with the error detection module, and configured to monitor a rate of error from the error detection module." Ex. 2 at claims 6, 7, 11, 12. And the specification puts the error monitoring module within a specific structure, the controller. *See id.* at 7:38-41.

The language of the claims would also evoke some specific structural aspects to a POSA. The error monitoring module is "communicatively coupled with the error detection module." Bagherzadeh Decl. ¶ 104; Ex. 2 at claims 6, 7, 11, 12. A POSA would recognize that an error monitoring module involves counting errors over a time period and would therefore include a digital "counter"—a known class of structures in digital circuit design to a person of skill. Bagherzadeh Decl. ¶ 105; Ex. 13, C.H. Roth, *Fundamentals of Logic Design* (2010) at Viasat_FEC_00003255-3260. The intrinsic evidence is consistent with this, describing the use of

digital counters for purposes of counting errors. Bagherzadeh Decl. ¶ 106; Ex. 14, U.S. Patent No. 6,751,766 at 13:40-49.

Finally, as with the other module terms in the asserted patents, Defendants statements to the Patent Office are entirely inconsistent with their proposed construction in this Court. In front of the PTAB, Kioxia identified what they say are error monitoring module structures in the prior art without raising any issue that such terms lacked a definite structure or were indefinite. *See, e.g.*, Ex. 3 at 43-47, 76-80. But apparently (and without explanation), the same term has become indefinite here.

H. The term "*the error detection module comprises the decoding module*" is neither nonsensical nor a logical impossibility

Western Digital's argument that the term "the error detection module comprises the decoding module" is indefinite rests on their mistaken assertion that the term does not make sense. Western Digital suggests the term presents a logical impossibility because (in its mistaken view) the error detection module must be fully distinct and separate from the decoding module if they are communicatively coupled. And therefore, the error detection module can never "comprise the decoding module."

Western Digital's argument ignores that claim 1, from which claim 14 depends, makes clear that being physically separate is something different than being communicatively coupled. Claim 1 requires that the error detection module be communicatively coupled **and physically separate** from the error correction module. Ex. 2 at claim 1. If Western Digital were correct that "communicatively coupled" necessitated physical separation, then the physically separate limitation would be superfluous, violating basic principles of claim construction. *See Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004) ("While not an absolute rule, all claim terms are presumed to have meaning in a claim."). By giving meaning

to all the words in the claim, it is evident that the decoding module and error detection module being "communicatively coupled" does not also require them to be separate or entirely distinct. For that same reason, the fact that the error detection module is "communicatively coupled" to the decoding module does not mean that it cannot also comprise the decoding module.

The term "the error detection module comprises the decoding module" is easily understood according to its plain and ordinary meaning without any further construction necessary. "Comprises" is a well-known patent term, and incorporating it here simply means the error detection module includes (without limitation) the decoding module. There is nothing complicated or nonsensical about the term.

IV. '347 Patent

A. "*Error correction sub-module*" is readily understandable as a definite structure according to its plain and ordinary meaning

For many of the same reasons as with the term "error detection sub-modules" and "error correction module" in the '700 patent, the term "error correction sub-module" in the '347 patent is easily understood by a POSA as describing a definite structure. *See* §§ III.B, III.D, *supra*. It requires no construction and can be understood according to its plain and ordinary meaning. A POSA readily and easily understands it is the structural component containing the circuitry on the chip (ASIC or otherwise) that corrects an error detected in a chunk of data read from the flash memory.[4] Bagherzadeh Decl. ¶ 76. No further construction is required.

Error correction sub-module is not a generic black box term that invokes means-plus-function claiming. The claim does not use the word "means" and is therefore presumed not to be

[4] As noted above in footnote 1, the distinction between an error correction module and sub-module creates no significant nuance or difficulty in their construction. A POSA would recognize according to their plain and ordinary meaning that an error correction module structure could be comprised of multiple error correction sub-modules. Bagherzadeh Decl. ¶ 77.

governed by § 112, ¶ 6. Defendants have not overcome that presumption, as neither the use of the word "sub-module" nor functional modifier language change the structural nature of the term. *See, e.g.*, *Zeroclick*, 891 F.3d at 1008.

As with the other "module" terms, the '347 patent's claims and specification provide additional language and context that "inform[s] the structural character" of the term error correction sub-module and illustrates its definite structure. *SAS Inst.*, 2020 WL 569856, at *15-16. Claims 1 and 13 describe the error correction sub-module as a structure that the system is, under certain conditions, "power[ed]-up, from an inactive mode." Ex. 15, U.S. Patent No. 8,966,347 at claims 1, 13. Functions are not powered up from an inactive mode; structures are. Bagherzadeh Decl. ¶ 91. Similar language describing the powering up or down of different error correction sub-module structures is replete in the specification as well. *See, e.g.*, Ex. 15 at Figs. 6 & 7, 1:49-52, 5:4-7, 5:18-20, 7:17-23. Additionally, the first and second error correction sub-module structures described in claims 1 and 13 are also described as being "arranged in parallel" with each other and shown as such in Figure 3 of the specification. Bagherzadeh Decl. ¶ 92; Ex. 15 at Fig. 3, claims 1 & 13. A POSA would recognize that error correction sub-modules that are arranged in parallel and selectively powered up are physical structures and not generic black box functions. Bagherzadeh Decl. ¶ 92. Finally, as discussed in Sections III.B and III.D, *supra*, the structural aspect of these terms is supported by the multiple statements in the specification (shared with the '700 patent) noting that these systems can be "implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware," as well as the discussion of using well-known error correction code algorithms reflective of physical structures in hardware such as ASICs. Bagherzadeh Decl. ¶ 94; Ex. 15 at 3:33-38, 4:9-30, 5:64-67.

A POSA would also recognize that the term error correction sub-module, in context of its parent error correction module, is a generally understood term in the art to describe a known class of structures that correct errors. Bagherzadeh Decl. ¶ 79; *Skky*, 859 F.3d at 1019. And a person of skill would understand that these error correction module structures could be composed of sub-modules, which would themselves be definite structures. Bagherzadeh Decl. ¶ 77; *see* Ex. 8 at Fig. 1; Ex. 5 at Fig. 1, Table II, Fig. 7; Ex. 6 at Fig. 5; Ex. 12 at Viasat_FEC_00002115.

And as noted above with the other module terms in the asserted patents, Western Digital has argued to the PTAB that this term requires no construction and instead may be understood according to its plain and ordinary meaning. *See* Sections III.B and III.D, *supra*. Western Digital's sudden inability to understand the structural nature of the term is suspect, given the many pages it spends locating those structures in the prior art. *See* Ex. 11 at 38-39, 44-49, 69-70, 71-73. The Court should not permit this kind of game playing.

But even if the Court finds the term error correction sub-module is governed by § 112, ¶ 6, the '347 patent discloses corresponding structures for the claimed function for the same reasons and based on the same disclosures as for error correction module. *See* § III.D, *supra*.

V. Conclusion

Viasat respectfully requests that the Court adopt its proposed constructions.

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Respectfully submitted,

/s/ *Melissa R. Smith*

Melissa R. Smith, State Bar No. 24001351
GILLAM & SMITH, LLP
303 South Washington Avenue
Marshall, Texas 75670
Telephone: (903) 934-8450
melissa@gillamsmithlaw.com

J. Scott McBride (*Pro Hac Vice*)
Matthew R. Ford (*Pro Hac Vice*)
Nevin M. Gewertz (*Pro Hac Vice*)
Tulsi E. Gaonkar (*Pro Hac Vice*)
BARTLIT BECK LLP
54 W. Hubbard Street, Suite 300
Chicago, IL 60654
Telephone: (312) 494-4400
scott.mcbride@bartlitbeck.com
matthew.ford@bartlitbeck.com
nevin.gewertz@bartlitbeck.com
tulsi.gaonkar@bartlitbeck.com

Nosson D. Knobloch (*Pro Hac Vice*)
Meg E. Fasulo (*Pro Hac Vice*)
BARTLIT BECK LLP
1801 Wewatta Street, Suite 1200
Denver, CO 80202
Telephone: (303) 592-3100
nosson.knobloch@bartlitbeck.com
meg.fasulo@bartlitbeck.com

Counsel for Plaintiff

CERTIFICATE OF SERVICE

I certify that on August 23, 2022, I electronically filed the foregoing with the Clerk of the Court using the CM/ECF System, which will then send a notification of such filing to counsel of record for Defendants.

/s/ *Melissa R. Smith*